AFFORDABLE OTM PHASED ARRAY ANTENNAS: DESIGN AND FABRICATION OF TEMPERATURE STABLE AND PERFORMANCE CONSISTENT PHASE SHIFTERS

M.W. Cole, W. D. Nothwang, C. Hubbard, E. Ngo, S. Hirsch
U.S. Army Research Laboratory, Weapons and Materials Research Directorate
Aberdeen Proving Ground, MD 21005, U.S.A.

L. A. Coryell
U.S. Army Communications& Electronics Research Development & Engineering Center
Space & Terrestrial Communications Directorate
Fort Monmouth, NJ 07703-5203, U.S.A.

ABSTRACT

Electronically scanned phased array antennas (ESAs) provide the means for achieving high data rate, beyond line of sight, on-the-move (OTM) communications. The phase shifter is a key component of ESAs, and the Army's Communications Engineering Research and Development Center (CERDEC) has recently acknowledged $BaSrTiO_3$ (BST) thin film technology as the premier candidate for achieving affordable high performance phase shifter elements. Unfortunately, there is concern that in practical applications the device performance will be compromised due to the temperature dependence of the BST based device capacitance. We report a material design which controls the magnitude and the sign of the temperature coefficient of capacitance (TCC) via a multilayer paraelectric BST/buffer layer/ferroelectric BST coplanar device structure. To realize this multilayer device structure we have designed, fabricated, and optimized an Al doped Ta_2O_5 barrier layer with low loss, moderate permittivity, low TCC, and excellent bias stability of capacitance. The integration of the barrier layer with the BST layers was optimized for structure, microstructure, interfacial/surface morphology, and dielectric properties as a function of Al doping concentration, annealing temperature, material growth and integration process parameters.

1. INTRODUCTION

Over the last decade $Ba_{1-x}Sr_xTiO_3$ (BST) has been investigated intensively for applications as tunable microwave devices, such as filters (Padmini etal., 1999; Miranda etal., 1997) and phase shifters (DeFlaviis etal., 1997; Chang etal., 2000; Park etal., 2000; Cole etal., 2002). For these tunable microwave devices, high dielectric tunability, low microwave loss, and good temperature stability are required for optimum performance and long-term reliability. The current generation of tunable microwave phase shifter devices is based on single composition, paraelectric BST films, and the military end-users have expressed significant concern that in practical applications, e.g., On-The-Move (OTM) phased array antennas, the phase shifter performance will be compromised due to the temperature dependence of the device capacitance (Coryell, 2004; Potenzaiani, 2005; Strimpler, 2005; Perlman etal., 2005). Specifically, the capacitance of the BST based device is strongly influenced by temperature changes because the dielectric constant (ε_r) of a single composition paraelectric BST films (e.g. $Ba_{0.5}Sr_{0.5}TiO_3$) follows the Curie–Weiss law;

$$K = C_{curie}/(T-\theta) \qquad (1)$$

where K is the dielectric constant, C_{curie} is the curie constant, T is the temperature, and θ is the Curie temperature (Jain etal., 2003). Spurious changes in the device capacitance that stem from ambient temperature fluctuations will disrupt the phase shifter performance via device-to-device phase shift and/or insertion loss variations leading to beam pointing errors and ultimately communication disruption and/or failure in the ability to receive and transmit the information. The same is true for BST based tunable filters where the capacitance susceptibility to temperature changes results in the alteration of the band pass window sharpness (window narrows or broadens), or the entire band pass window may shift to higher or lower frequencies and/or the insertion loss may be degraded. Such poor temperature stability of the capacitance would result in the carrier signal drifting in and out of resonance on hot and cold days.

Traditional approaches to address the issue of device (phase shifter and/or tunable filter) temperature instability have focused on employing hermetic or robust packaging, whereby the robust package serves to protect the tunable device from the harsh environmental extremes. Although this approach is successful, hermetic/robust packaging would add significant cost, size, and weight to these OTM phased array antennas, which in turn violates the military and commercial sectors requirements for affordability. It is not foreseeable that such an approach could meet the criteria of a low cost phase shifter i.e. ~$5.00 per phase

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
01 NOV 2006	**N/A**	**-**

4. TITLE AND SUBTITLE
Affordable Otm Phased Array Antennas: Design And Fabrication Of Temperature Stable And Performance Consistent Phase Shifters

5a. CONTRACT NUMBER
5b. GRANT NUMBER
5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)

5d. PROJECT NUMBER
5e. TASK NUMBER
5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
U.S. Army Research Laboratory, Weapons and Materials Research Directorate Aberdeen Proving Ground, MD 21005, U.S.A.

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR’S ACRONYM(S)

11. SPONSOR/MONITOR’S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release, distribution unlimited

13. SUPPLEMENTARY NOTES
See also ADM002075., The original document contains color images.

14. ABSTRACT

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**UU**	**8**	

shifter element (Coryell, 2004). Other concepts to achieve temperature stability compliance, involve the use of "system heat sinks" and/or cooling apparatuses such as "mini fans" and/or "temperature compensation circuits" or "mini ovens-heating units". Such thermal management solutions (fans/heat sinks/ovens and various other types of thermal management) may be utilized with the OTM antennas; however they will add extra weight, size, and cost to the overall system, and as such, are deemed unacceptable. Temperature compensation can also be achieved using either the (1) curve fit or (2) look up table approach. The curve fit approach centers on the formulation of a temperature dependant mathematical expression/equation, which represents the drift of each BST tunable device. A microprocessor utilizes this equation and the ambient temperature data (obtained from a thermocouple mounted on the printed circuit board) to calculate the tuning voltage. The look-up table approach, as its name implies involves using a look up table. In order to obtain the look-up table coefficients, the phase shifter characteristics must be measured at discrete temperatures then the BST bias voltage is manually adjusted to maintain the phase shifter specifications. In the worst-case scenario, one would have to obtain a set of points for each temperature (i.e., 23 ^{o}C, 24 ^{o}C etc.). Typically one would expect to have a small subset of temperature/bias points for each bias line. The exact number of points is of course dependent on the BST devices, the other phase shifter components, and the phase shifter topology. Unfortunately, this approach can be quite complex as there usually isn't a one size fits all solution. The calibrations are also labor and time intensive and are useful if only a limited number of OTM phased array antennas are to be fielded. Common-place materials science approaches for reducing the temperature dependence of an active material have been to select the temperature interval of operation well above the temperature corresponding to the active materials permittivity maximum. Unfortunately, this method results in reduced material tunability and the temperature coefficient of capacitance (TCC) is still too high for practical military applications such as OTM phased array antennas.

(a)

(b)

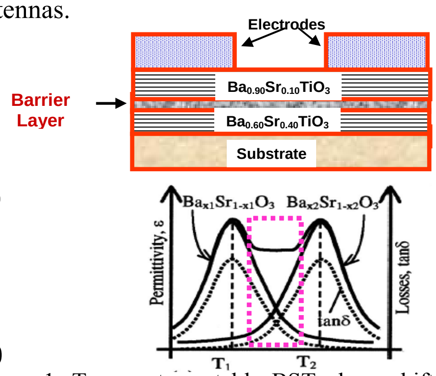


Figure 1. Temperature stable BST phase shifters: (a) the thin film tri-layered, BST/barrier-layer/BST material design and (b) the expected material response.

Our approach for BST device temperature compensation is based on the thin film device concept shown in Figure 1. This design employs a tri-layer (paraelectric BST/buffer layer/ferroelectric BST) material structure which aspires to lower the TCC of the film whereby each BST thin film is designed with a distinct dielectric response (Curie temperature) over a specified temperature range, T_1 and T_2 (T_1 and T_2 correspond to the systems temperature specifications). Thus, the phase shifter consists of two BST thin films with different Curie temperatures where one is in the paraelectric phase ($Ba_{0.60}Sr_{0.40}TiO_3$) and the other is in the polar phase/ferroelectric ($Ba_{0.90}Sr_{0.10}TiO_3$) in the application temperature interval if interest, T_1 and T_2. In the temperature interval between the two curie peaks (T_1 and T_2), the permittivity of the polar phase increases with increasing temperature, while the permittivity of the paraelectric phase decreases. Thus in a phase shifter, where these two phases are connected in parallel the decreased permittivity of the paraelectric phase is compensated by the increased permittivity of the ferroelectric phase. The device geometry, the temperature interval T_1 and T_2, and the material compositional design can be adjusted to possess the desired TCC to meet the systems temperature performance specifications. In order to realize this device design a "passive/non-tunable", temperature stable, microwave friendly dielectric thin film barrier layer must be developed, optimized and integrated with the active BST thin films. The barrier layer is fundamental to the device design as it is sandwiched between the two BST films in order to prevent chemical interaction, i.e., serves to prevent the formation of a new BST phase between the two BST films, and to ensure distinct maximums of the dielectric permittivity for the two BST films. In this paper we report on the growth, process science, optimization, and integration of the Al-Ta_2O_5 thin film barrier layer to enable the realization of the temperature insensitive tri-layer film device design shown in Figure 1.

2. EXPERIMENT

The experiment consisted of two parts; (1) fabrication and optimization of the Al-doped Ta_2O_5 buffer layer and (2) developing the integration strategy to achieve the tri-layerd film device configuration schematically displayed in Figure 1. The experimental methodologies are described below:

The Al-Ta_2O_5 buffer layer thin films were fabricated via the metalorganic solution deposition (MOSD) technique. In the MOSD process tantalum ethoxide was used as the precursor to form the Ta_2O_5 film. Acetic acid and 2-methoxyethanol were used as solvents, and Al-nitrate was employed as the dopant in the concentration range from 1 to 20 mol%. The stoichiometric precursor solutions were

concentration optimized for solution viscosity and spin coated onto Pt-coated silicon (PtSi) substrates. Particulates were removed from the solution by filtering through 0.2 mm syringe filters. Subsequent to coating the films were pyrolyzed at 350 °C for 10 min. in order to evaporate solvents and organic addenda and form an inorganic amorphous film. The spin coat pyrolization process was repeated until the desired nominal film thickness (100 nm) was achieved. Crystallinity was optimized via postdeposition annealing at temperatures ranging from 600 to 800 °C (depending on Al doping concentration) in an oxygen ambience for 60 min. The crystallinity and surface morphology of the films were assessed by glancing angle x-ray diffraction (GAXRD) and atomic force microscopy (AFM) using a Rigaku diffractometer with Cu *K*a radiation at 40 kV and a Digital Instruments Dimension 3000 tapping mode AFM, respectively. A Hitachi S4500 field emission scanning microscope (FESEM) was utilized to assess the cross-sectional and plan-view film microstructure. The electrical measurements, i.e., the dispersion of dielectric response (capacitance and loss tangent) of the Al doped Ta_2O_5 thin films was measured as a function of frequency (1 kHz to 1 MHz), temperature (25-125 ^oC) and applied bias (-20 to +20 V) in the metal-insulator-metal (MIM) device configuration using Pt as the bottom and top electrodes. The film capacitance (C_p) and dissipation factor (tan δ) were measured with an HP 4194A impedance/gain analyzer. The insulating properties of the films were evaluated via I-V measurements using a HP 4140B semiconductor test system from 0.1-1.0 MV/cm.

Subsequent to the optimization of the Al-doped Ta_2O_5 thin film the tri-layer integrated coplanar device was achieved via a tri-deposition-anneal process science protocol. Specifically, 230 nm $Ba_{60}Sr_{40}TiO_3$ (BST 60/40) paraelectric film was deposited onto the PtSi substrate, pryrolyzed at 350 ^oC and postdeposition annealed in an oxygen ambience for 60 min at 750 ^oC. The experimental details of details of the BST film fabrication have been presented elsewhere (Cole etal., 2000; 2003). Next, 100 nm of Al-doped Ta_2O_5 was MOCVD deposited, pryrolyzed at 350 ^oC, and anneal optimized at 750 ^oC for 60 minutes. Subsequent to the Ta_2O_5 film anneal a 230 nm ferroelectric $Ba_{90}Sr_{10}TiO_3$ (BST 90/10) film was MOSD deposited over the Al-doped Ta_2O_5 film. The composite tri-layer structure was subjected to a final anneal for 60 min. at 750 ^oC in an oxygen ambiance.

3. RESULTS AND DISCUSSION

For a thin film inter-layer to be useful as a buffer layer in the device design concept shown in Figure 1, i.e., integrated with the paraelectric and ferroelectric active BST thin films, several material property requirements must be satisfied. Specifically the candidate buffer layer film must have a low temperature coefficient of capacitance (TCC); possess good bias stability (i.e. be passive/non-tunable); the film must be microwave friendly, i.e., possess low dielectric loss, moderate permittivity, low leakage current; the buffer film must have good adhesion to underlying paraelectric BST film and possess a smooth crack free surface morphology to allow good adhesion with the overlying ferroelectric BST film; the buffer film must possess a crystalline dense microstructure with a single phase structure and minimum defects; the film must be refractory at the BST annealing temperature (750 ^oC) such that the buffer film would withstand BST processing conditions without interdiffusion; and the buffer layer film must possess large area uniform material properties and these material properties must be reproducible via industry standard processing protocols.

The buffer layer thin film is critical to the overall material temperature stable phase shifter design and as such its fabrication, characterization and optimization must be achieved preceding its integration into the device structure shown in Figure 1. Thus, prior to the integration of the Al-doped Ta_2O_5 films into the tri-layer BST/buffer layer/BST device structure the Al-doped Ta_2O_5 films were optimized as a function of doping concentrations and annealing conditions. The as-pyrolyzed Al-Ta_2O_5 MOSD fabricated films were amorphous in nature and postdeposition annealing was required to obtain fully developed crystalline films, increase the overall grain size of the film, and to remove film strain by filling oxygen vacancies. GAXRD analysis was employed to access the influence of Al doping concentration on the crystallization temperature (Figure 2). The GAXRD results displayed in Figure 2 clearly demonstrates that as the concentration of Al doping increases the demand for enhanced crystallization temperatures also increases. Specifically, films Al doped $\leq$ 5 mol% were anneal optimized at a crystallization temperature of >650 ^oC, films doped 10 mol% were anneal optimized at $\geq$700 ^oC (i.e., 750 ^oC), and films doped from 15-20 mol% required annealing temperatures of 800 ^oC to achieve full crystallinity. The GAXRD results demonstrated that the anneal-optimized Al doped films were well-crystallized, single phase, orthorhombic in structure with a preferential (200) orientation.

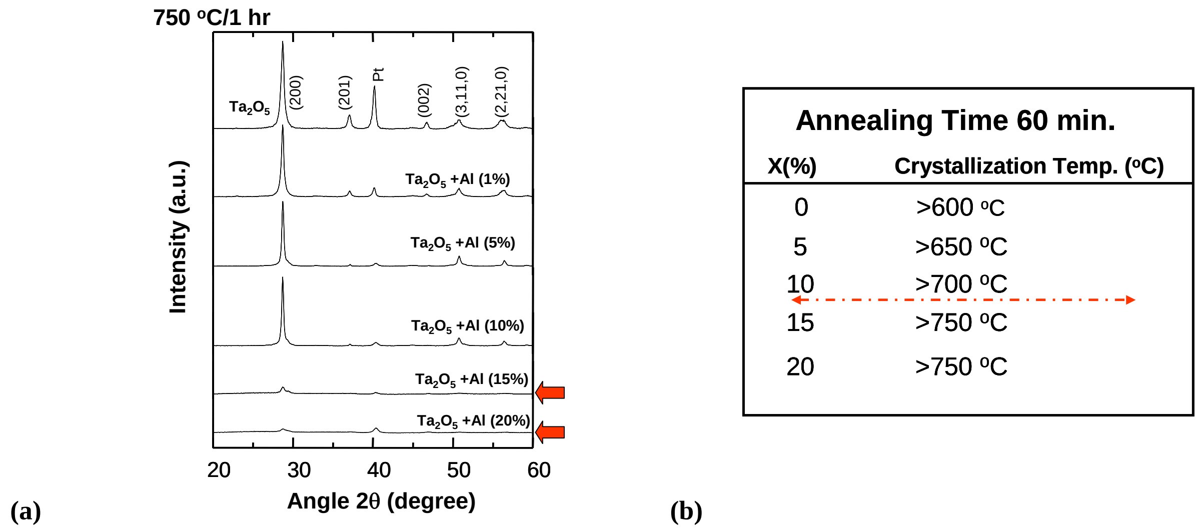


Figure 2. Structural analysis of Al doped Ta_2O_5 films annealed for 60 min at 750 °C (a) the GAXRD patterns for the 1-20 mol % Al doped films and (b) the minimum annealing temperature required to crystallize the films as a function of Al doping concentration.

Table I: Dielectric properties of (1-x)Ta_2O_5-xAl thin films as a function of annealingTemperature (T_A).

Al dopant (mol %)	**T_A=700°C**		**T_A=750°C**		**T_A=800°C**	
	ε_r	**t an δ**	ε_r	**tan δ**	ε_r	**tan δ**
0	50.4	0.007	51.7	0.008		
5	39.7	0.011	42.8	0.005		
10	24.8	0.009	42.8	0.005		
15	24.0	0.007	27.0	0.007	40.6	0.009
20	21.0	0.006	25.0	0.006	44.6	0.009

Table II: The leakage current density, temperature coefficient of capacitance (TCC) and bias stability of the Ta_2O_5 thin films as a function of Al dopant concentration.

Al dopant (mol %)	**J_L (A/cm^2) 1 MV/cm Amorphous**	**Crystalline**	**TCC (ppm/°C) (25-125 °C)**	**Bias Stability C_p(%) up to 1 MV/cm**
0	<2.2e-10	<4.5e-7	+114	1.41
5	<3.0e-10	<5.9e-8	+24	0.76
10	<2.0e-10	<3.4e-8	-20	0.40
15	<3.2e-10	<3.0e-8	-58	0.23
20	<7.2e-10	<4.3e-9	-48	0.24

Table I displays the dielectric response of the buffer layer films as a function of Al doping concentration and annealing temperature. The permittivity and dielectric loss of the films with Al doping levels up to 10% mol % achieved their lowest loss and highest permittivity values after annealing at 750 °C for 60 min. The 15 and 20% Al doped films achieved their optimum dielectric response after annealing at 800 °C, however this elevated temperature is in excess of that required for reliable integration within the BST/buffer layer/BST tri-layer device structure shown in Figure 1 and as such cannot be utilized for the device concept. The results tabulated in Table I suggest that the 10 mol% Al doped Ta_2O_5 possess the best dielectric properties, i.e., the low dielectric loss and high permittivity, for utilization as a buffer layer in the temperature stable phase shifter device design concept.

For Al-Ta_2O_5 films to be of practical use as an integration barrier layer for temperature stable phase shifting devices the film must possess low leakage, and minimal dielectric dispersion with both temperature and applied bias. Table II displays the leakage current density, temperature coefficient of capacitance (TCC) and bias

stability data for the Al doped Ta_2O_5 thin films. The temperature coefficient of capacitance was calculated via equation (2)

$$TCC = \Delta C/(C_o \Delta T) \qquad (2)$$

whereby, ΔC is the change in capacitance with respect to C_o at 25 ^oC and ΔT is the chance in temperature relative to 25 ^oC. The bias stability of capacitance as a function of Al doping is also displayed in table II. The bias stability of capacitance is calculated from equation (3)

$$Cp = [C_{(1MV/cm\ bias)} - C_{(no\ bias)}]/\ C_{(no\ bias)} \qquad (3).$$

The results in Table II demonstrate that 750 ^oC anneal optimized 10 mol % Al doped films exhibited the lowest leakage characteristics (~10^{-8}A/cm^2). Leakage current is one of the limiting characteristics of a dielectric material for microwave device applications. The leakage current density of the thin film as a function of applied electric field is an electrical measure of the quality and reliability of a dielectric film (Cole etal., 2000, 2003; Saha and Krupanidhi, 2000). Elevated leakage current values suggest poor device reliability and ultimate device failure/breakdown. The low leakage current (<3.4e-8 **A**/cm^2 1 at MV/cm) observed for the 10 mol% Al doped film demonstrates the completeness of phase formation and oxidation of the 10 mol% Al doped Ta_2O_5 MOSD fabricated thin film. The leakage current was observed to increase slightly with applied electric field (up to 1 MV/cm). It has been suggested that at high fields, grain boundary conduction may be larger than the grain conductivity setting large tunneling currents through these grain boundary layers. However even at these large field strengths the MOSD fabricated 10 mol% Al doped Ta_2O_5 film possessed excellent leakage characteristics. The 10 mol% Al doped film also possessed the lowest TCC (-20 ppm/^{o}C) deeming it temperature stable from over the temperature range of 25 to 125 ^oC.

To be utilized as a barrier layer the Al-doped film must not be tunable, i.e. it should be passive and exhibit good bias stability characteristics. Poor bias stability of the buffer layer would interfere with the tunability of the active BST material in the device and in turn would result in extreme unpredictable and uncorrectable errors in antenna phase shift. Such unexpected phase shift modifications would disable the antenna's ability to receive and/or transmit the information and ultimately result in communication failure. Therefore, it is necessary for the buffer layer component (Al-Ta_2O_5) of the phase shifting element to be bias insensitive. The bias stability of capacitance (Table II) was observed to decrease with increasing Al concentration up to 10 mol% however; the lowest values were observed for the 15-20 mol% Al doped films which displayed bias stability of capacitance saturation at ~ 23.5 %. Since the 15 and 20 mol% films are considered long term reliability "risks" the 10 mol% Al doped Ta_2O_5 film is considered the to possess the lowest value of bias stability of capacitance, (0.4% at 1 MV/cm) and is classified as non-tunable or passive with applied bias. Figure 3a shows that the capacitance and dissipation factor for the 10 mol% Al doped Ta_2O_5 barrier film exhibited negligible dispersion as a function of applied bias from 20 to -20 V. Specifically, The loss factor possessed excellent bias stability, i.e., less than 1% up to 1 MV/cm. The dielectric permittivity and dissipation factor of the 10 mol % Al doped Ta_2O_5 thin film as a function of frequency is shown in Figure 3b. The small signal dielectric constant and dissipation factor at a frequency of 100 kHz were 42.8 and 0.005, respectively. The permittivity and loss factor showed no appreciable dispersion with frequency up to about 1 MHz indicating that the values were not masked by any surface layer effects or electrode barrier effects in this frequency range. Thus, based on the excellent dielectric properties, the frequency and bias stability the 10 mol% Al doped Ta_2O_5 film is considered to be the most favorable barrier layer candidate for realizing the temperature stable phase shifting device in OTM antennas.

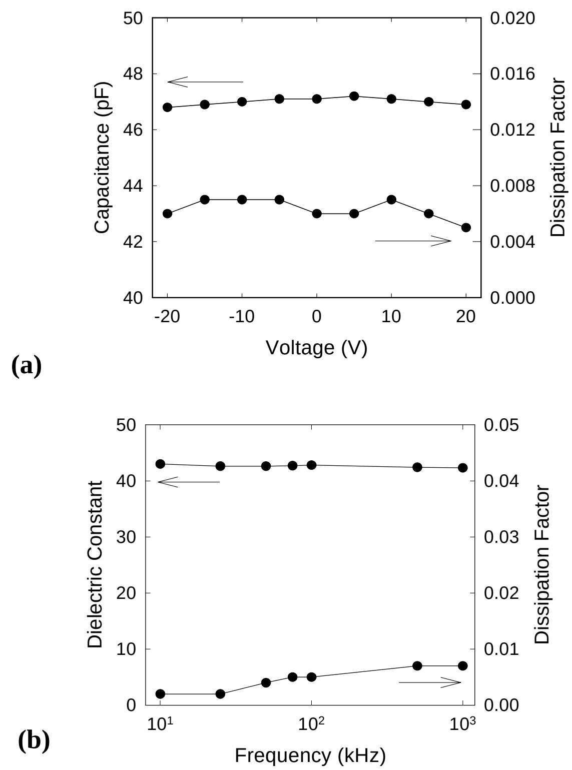
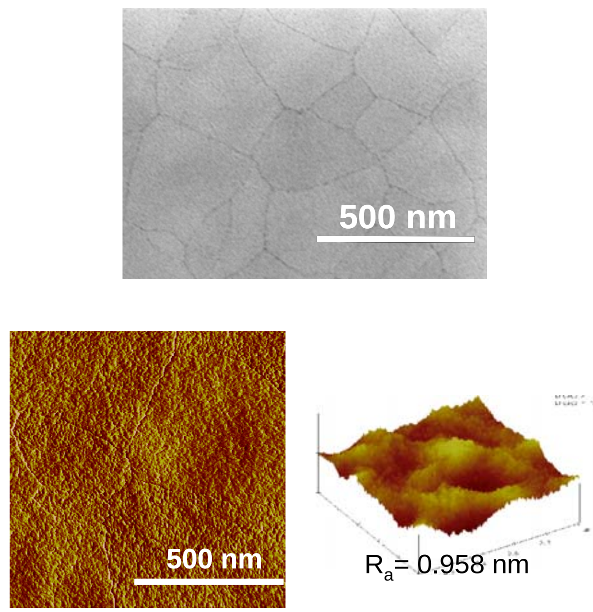


Figure 3. Dielectric dispersion of the 10 mol % Al doped Ta_2O_5 thin film: (a) the capacitance-voltage and dissipation-voltage characteristics from -20 to +20 volts and (b) the dielectric permittivity and dissipation factor as a function of frequency from 10 to 1000 kHz.

In conjunction with the dielectric and insulating properties discussed above there are other materials properties, which must be satisfied for Al doped -TaO_5 to be a successful candidate as a buffer layer in phase shifting devices. For a buffer layer film to be monolithically integrated between the underlying and overlying BST active thin films to realize the tri-layer device structure depicted in Figure 1 the buffer film must possess a pristine, surface morphology. In other words, a smooth, continuous, uniform, defect free surface morphology of the Al-Ta_2O_5 film is critical if it is to serve as the "pseudo-substrate" for the growth of the overlying ferroelectric BST (90/10) active layer in the coplanar device configuration. If the Al-Ta_2O_5 film surface is not smooth a rough buffer layer-BST film interface will result, and this interfacial roughness will in turn promote a rough BST film surface. In a coplanar microwave device design the top surface of the BST film must be metallized in order to fabricate the electrodes, i.e., the ground and center conductors of the device (Figure 1). There are losses associated with the electrode metallization and a rough film-metal electrode interface will augment the overall loss of the device (Cole etal., 2002). Minimization of film-metal interfacial roughness serves to reduce the conductor loss and improves the overall device loss for microwave frequency operation. Thus, the quality of the conductor-BST film interface is critical, and is strongly dependent on the nature of the buffer layer's surface morphology. Plan-view FESEM and AFM analyses were utilized to evaluate the 750 ^{o}C annealed 10 mol % Al doped Ta_2O_5 film surface for feasibility of promoting the growth of a continuous BST film/over-layer with a uniform/smooth defect free surface morphology. The plan-view FESEM and AFM images are displayed in Figure 4. The micrographs show that the buffer film exhibited a smooth uniform microstructure with no cracks or defects observed. Furthermore, the AFM results demonstrated that the 10 mol% Al-Ta_2O_5 film possessed a dense microstructure composed of 200 nm domains, which encases a fine grain nano-crystallite microstructure or subgrains, with a grain size on the order of 25 nm. This domain-type microstructure is most visible in the plan-view FESEM micrographs of the film surfaces (Figure 4a). The average surface roughness of the 750 ^{o}C post-deposition annealed films, as quantified by AFM, was found to be <1 nm. Thus, the 10 mol% Al doped Ta_2O_5 film surface properties, i.e., extreme uniformity, smoothness, and defect free nature, appear to be well suited for the BST overgrowth.

Subsequent to the optimization of the Ta_2O_5 buffer layer film the challenge of integrating the buffer layer with the active BST thin films was addressed. To accomplish the integration task a tri-deposition/anneal process science protocol was employed whereby each layer of the tri-layer film device structure was annealed prior to the deposition of the overlying film. The individual film anneals were required to keep the film interfaces smooth abrupt and defect free. As mentioned previously, the quality of the film interfaces directly influences the surface morphology of the final device structure, which, in turn, influences the magnitude of conductor loss associated with the metal contacts of the coplanar device. The surface morphology of the integrated tri-layer device structure must be continuous, smooth, uniform, and crack/defect free. Figure 4 displays the AFM images of the integrated film structure (BST/buffer layer/BST) surface morphology. The surface morphology exhibited a dense microstructure with no cracks or defects observed and the surface roughness (Figure 4b) as quantified by AFM, was 1.7 nm.

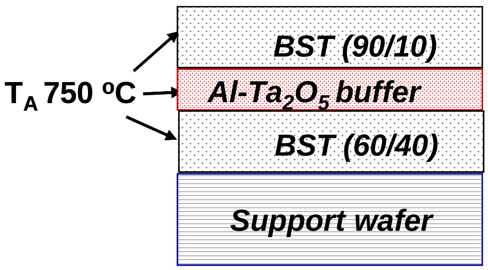


(a)

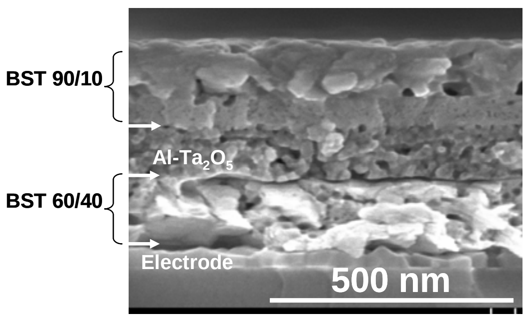
(b) (c)

Figure 4. Surface morphology of the 750 ^{o}C annealed 10 mol% Al-Ta_2O_5 thin film; (a) FESEM plan-view image, (b) AFM plan-view and (c) 3-D AFM images.

The cross-sectional FESEM micrograph of the tri-deposition/anneal device structure is displayed in Figure 5. The FESEM results demonstrate that the constituent films possessed a dense well-crystallized microstructure with uniform thickness. The FESEM micrograph shows a distinct structural delineation between the layered films and with the PtSi substrate. No amorphous layer or void/defects were observed at the interfaces. The excellent crystallinity, defect free structurally abrupt interfaces in concert with an extremely smooth, uniform and defect free surface morphology bodes well for the integration suitability of this tri-layer device structure fabricated via a tri deposition/anneal process science protocol.



(a)



(b)

Figure 5. The tri-deposition/anneal integration process science protocol: (a) schematic and (b) the cross-sectional FESEM micrograph showing the paraelectric BST/Al-Ta_2O_5/ferroelectric BST integrated tri-layer device structure.

CONCLUSIONS

This investigation demonstrated the feasibility of utilizing MOSD fabricated Al doped Ta_2O_5 as a buffer layer film to promote temperature stable BST based phase shifter devices. The buffer film's material properties were evaluated as a function of Al dopant concentration (1-20 mol%) and annealing temperature. Our results deemed the 750 ^oC annealed 10 mol% Al doped Ta_2O_5 film to be the best candidate for the temperature stable phase shifter device buffer layer. The 750 ^oC anneal optimized 10 mol% Al doped Ta_2O_5 based thin film possessed excellent material properties, namely, an enhanced dielectric constant (ε_r =42.8), low dielectric loss (tan δ=0.005), low leakage characteristics (3.4x10^{-8} A/cm^2 at E=1 MV/cm), excellent temperature stability (TCC of -20 ppm/^{o}C), and excellent bias stability of capacitance (~0.06% at 1 MV/cm). Additionally, the permittivity and dissipation factor exhibited minimal dielectric dispersion with frequency, temperature, and applied bias. The optimized dielectric passive buffer layer film was typified by a uniform dense microstructure with minimal defects, and a smooth, nano-scale fine grain, crack/pinhole free surface morphology. The integration of the 10 mol% Al doped Ta_2O_5 buffer film with the paraelectric and ferroelectric active BST bilayer (in the coplanar device configuration), was demonstrated via a tri-deposition/anneal fabrication process science protocol. This integration process protocol promoted fully crystallized discrete BST/buffer layer/BST thin films (i.e., no evidence of interdiffusion), with defect free, structurally abrupt multi-layer film interfaces. Our results suggest that it is the combination of material design, film processing science, and the anneal optimized integration process protocol that allowed the successful realization of the tri-layer BST (60/40)/Al-Ta_2O_5/BST (90/10) temperature stable coplanar phase shifter device structure. In addition to developing this temperature stable phase shifter device, our work also served to ensure phase shifter device affordability by utilizing film fabrication and integration technology protocols that are industry standard i.e., compliant with current CMOS process science methods and materials. The impact of this materials integration technology will promote broad scale implementation of affordable On-The-Move phased array antenna systems across a variety of advanced communications platforms.

REFERENCES

Chang, W. , Horwitz, J. S. , Carter, A. C., Pond, J. M. , Kirchoefer, S. W. , Gilmore, C. M.and Chrisey, D. B. Appl. Phys. Lett. **74**, 1033 (2000).

Cole, M.W., Joshi, P.C. , Ervin, M.H., Wood, M.C. and Pfeffer, R.L Thin So**74**, 34 (2000).

Cole, M. W., Hubbard, C., Ngo, E., Ervin, M., Wood, M. and Geyer, R. G. J. of Appl. Phys. **92**, 475 (2002).

Cole, M.W., Nothwang, W.D., Hubbard, C. , NgO, E. and Ervin, M. J. of Appl. Phys. **93**, 9218 (2003).

Coryell, L., private communication CERDEC, Ft Monmouth NJ (2004).

De Flaviis, Alexopoulos, N. G. and Staffsudd, M., IEEE Trans. Microwave Theory Tech. **45**, 963 (1997).

Jain, M. , Majumder, S.B., Katiyar, R. S., Miramda, F. A. and Van Keuls, F. W. Appl. Phys. Lett. **82**, 1911 (2003).

Miranda, F. A., Romanofsky, R. R., Van Keuls, F. W. , Mueller, C. H., Treece, R. E. and Rivkin, T. V., Integr. Ferroelectr. **17**, 231 (1997).

Padmini, P, Taylor, T. R., Lefevre, M. J., Nagra, A.S., York, R.A. and Speck, J. S. Appl. Phys. Lett. **75**, 3186 (1999).

Park, B. H., Gim, Y., Fan, Y., Jia, Q. X., and Lu, P.. Appl. Phys. Lett. **77**, 2587 (2000).

Perlman, B. [CERDEC, Ft. Monmouth, NJ] L. Katehi, A. Ballato [CERDEC] , D. Peroulis, W. Chappell, Presentation at the 2005 U.S. Army Workshop "*Advanced Active Thin Film Materials For The Next Generation Of Meso - Micro Scale Army Applications*", Hilton Sandestin Beach Golf Resort & Spa Destin, FL, and May 10-12 (2005).

Potenziani, E. [CERDEC Intelligence and Information Warfare Directorate] Presentation at the 2005 U.S. Army Workshop "*Advanced Active Thin Film Materials For The Next Generation Of Meso - Micro Scale Army Applications*", Hilton Sandestin Beach Golf Resort & Spa Destin,FL, May 10-12, (2005).

Saha, S. and Krupanidhi, K.B., J. Appl. Phys. **87**, 3056 (2000).

Strimpler C, [CERDEC STCD] Presentation at the 2005 U.S. Army Workshop "*Advanced Active Thin Film Materials For The Next Generation Of Meso - Micro Scale Army Applications"* , Hilton Sandestin Beach Golf Resort & Spa Destin, FL, May 10-12, (2005).